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Abstract

Modern multicore processors have the potential to provide raw computing power while being energy-efficient and cost-effective. While many of the systems have already deployed multicore processors for their operation, their adoption in time-sensitive applications is still active research. The main reason behind this is the architecture of a typical multicore processor. The typical architecture used in COTS platforms makes use of shared resources such as shared system bus, main memory, shared caches, etc., among all/several cores. A task can suffer inter-core interference from the co-running tasks while accessing these shared resources. This inter-core interference can impact the temporal behavior of the tasks and analyzing the worst-case timing behavior of a task becomes extremely challenging. The 3-phase task model was proposed to circumvent this problem by dividing the execution of each task into memory and execution phases. In the 3-phase task model, the memory accesses can only happen during a memory phase and a core can execute a memory phase while other cores are busy executing the execution phases. Even though some existing approaches focus on analyzing the schedulability of the 3-phase task model under partitioned scheduling, several open issues exist. In this paper, we identify the key open issues that are important to address in order to derive the schedulability analysis for the 3-phase task model using partitioned scheduling.

Open Issues in Analyzing the Schedulability for the 3-Phase Task Model using Partitioned Scheduling

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Abstract
Modern multicore processors have the potential to provide raw computing power while being energy-efficient and cost-effective. While many of the systems have already deployed multicore processors for their operations, their adoption in systems that run time-sensitive applications is still active research. The main reason behind this is the architecture of a typical multicore processor. The typical architecture used in commercial-off-the-shelf (COTS) platforms makes use of shared system bus, main memory, shared caches, etc., among all/several cores. A task can suffer inter-core interference from the co-running tasks while accessing these shared resources. This inter-core interference can impact the temporal behavior of the tasks and analyzing the worst-case timing behavior of a task becomes extremely challenging. The 3-phase task model was proposed to circumvent this problem by dividing the execution of each task into memory and execution phases. In the 3-phase task model, the memory accesses can only happen during a memory phase and a core can execute a memory phase while other cores are busy executing the execution phases. Even though some existing approaches focus on analyzing the schedulability of the 3-phase task model under partitioned scheduling, several open issues exist. In this paper, we identify the key open issues that are important to address in order to derive the schedulability analysis for 3-phase tasks scheduled using partitioned scheduling.

Author Keywords. Multicore Platforms, Schedulability Analysis, Partitioned Scheduling, Bus Contention, Memory Contention.

1. Introduction

Multicore processors were introduced to meet the increasing demand for computing power, energy-efficiency, and cost-effective solutions. Many devices such as mobile phones, computers, smart TV, etc. have integrated multicore processors in their designs in order to take advantage of these features. However, the use of multicore platforms in systems that run time-sensitive applications such as avionics, automotive, railways, etc. is under scrutiny of the real-time systems research community. The main reason is that COTS multicore platforms have shared resources such as system bus, shared cache, main memory, etc. that are shared between the cores. Due to such architectural design, a task running on a given core may suffer inter-core interference from the tasks running on other cores (co-running tasks) while accessing these shared resources. This inter-core interference is dependent on specific properties of co-running tasks such as the number of memory requests, maximum time required to serve each memory request, type of memory request, etc.

The 3-phase task model [1,2] was introduced to reduce the unpredictability caused by the shared resource accesses in COTS multicore systems. In the 3-phase task model, the execution of each task is divided into three phases, i.e., *Acquisition* (A), *Execution* (E), and *Restitution* (R) phases. A task fetches the data from the main memory by accessing the system bus and loads it in the core's local memory during the A-phase. During the E-phase, the core executes the

task by accessing the data available in the core's local memory. Finally, during the R-phase, the task writes-back the modified data to the main memory by accessing the system bus. Consequently, A- and R-phases are considered memory phases whereas the E-phase is the execution phase. In the 3-phase task model, a core can execute a memory phase without suffering the inter-core interference when other cores are executing the execution phases.

2. Problem Definition

Even though the 3-phase task model can reduce the temporal unpredictability in multicore systems, tasks can still suffer inter-core interference in some scenarios. Such a scenario happens when tasks running on different cores want to execute a memory phase at the same time. Since the system bus is responsible to connect all the cores with the main memory, there can be a scenario in which a task wants to access the system bus while the system bus is busy handling the memory phase of co-running tasks. This phenomenon is known as bus-contention. Similarly, tasks can suffer inter-core interference at the main memory when the main memory is serving the memory requests of co-running tasks. This phenomenon is known as memory-contention. The problem of bus-contention and memory-contention in the 3-phase task model can negatively impact the temporal behavior of the tasks. Therefore, it is necessary to compute the upper-bound on the bus-contention and memory-contention to safely derive the schedulability analysis for 3-phase tasks.

3. State-of-the-Art

Works like [3] proposed a fine-grained bus-contention analysis for the 3-phase task model using fixed-priority partitioned scheduling. The bus blocking analysis is formulated by considering the set of memory phases running on the core under analysis and on all the other cores.

On the other hand, works like [4] compute the main memory-contention that can be suffered by the 3-phase tasks under partitioned scheduling. Such analysis accounts for the type of memory request (i.e., read or write), number of memory requests, and locality of the requested memory block in the main memory. By integrating the maximum memory-contention suffered by the 3-phase tasks, the memory-aware response time analysis is formulated for fixed-priority partitioned scheduling.

4. Open Issues

Even though the above-mentioned works focus on the schedulability analysis for the 3-phase tasks under partitioned scheduling, the following open issues still exist:

- **Open Issue 1:** Casini et al. [4] proposed a fine-grained analysis to compute the main memory-contention suffered by the 3-phase task using partitioned scheduling. However, their approach assumes a specific architecture that has a cross-bar switch that is responsible for point-to-point communication between the cores and the main memory. Thus, it ignores the problem of bus-contention that can be suffered by a task from co-running tasks due to the shared system bus accesses. This limits the applicability of [4] to only certain multicore architectures.
- **Open Issue 2:** The bus blocking analysis proposed in [3] assumes that the bus arbitration policy is First-Come First-Served (FCFS). Such an assumption limits the work of [3] to a certain bus arbitration policy. It is not known whether such analysis can be directly applied to multicore platforms that employ different bus arbitration policies such as processor-priority, round-robin, TDMA, etc. Furthermore, their approach does

not account for the worst-case time taken by the main memory to serve each memory request on the basis of type of request, location of requested memory block, etc.

Addressing the above-mentioned open issues is important because it will allow to derive a safe bound on the worst-case response time for the 3-phase task model under partitioned scheduling. However, addressing the above-mentioned open issues can be extremely challenging due to the complexity of the problem. For instance, the complexity can significantly increase while holistically analyzing the impact of bus-contention and memory-contention under the same framework.

5. Conclusion

In this work, we briefly discuss the problem of bus-contention and memory-contention that can be suffered by the 3-phase task model in fixed-priority partitioned scheduling. We further identified the open issues that have not been addressed in the state-of-the-art, their importance and possible challenges.

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